X80200 Triple Voltage Sequencer Basics: Examples of Various Power Sequencing Solutions

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Introduction

There is often a need in systems to provide power supply sequencing. This may be due to power supply turn on and off restrictions on the processor or DSP. Or, there could be a need to manage loads on power-up or to control the turn on sequence of peripheral devices. These requirements can lead to complicated and expensive solutions.

The X80200 Triple Voltage Sequencer is a device that simplifies the design of point of load power sequencing solutions. It is a highly flexible device that reliably connects up to three separate power supplies to their load by controlling individual MOSFETs. With built in charge pumps, the X80200 drives N-Channel FETs, providing minimum voltage loss and highest efficiency, even when controlling very low voltages.

The X80200 has two modes of operation, one that uses voltage feedback to control sequence timing and one that uses internal timers. In addition, the X80200 provides core up first, core down last logic that provides protection for those devices that must have the proper core voltage applied before the I/O voltage turns on and must remove the I/O voltage before the core voltage fails.

This application note explores some of the ways that the X80200 can be connected to provide virtually any power supply turn on sequence. The examples provided are all tested using the X80200 Evaluation Kit from Intersil.

X80200 Operation

The X80200 device controls the output sequence of power supplies, regardless of their initial power-up sequence, by:

- monitoring the input voltages to ensure they are all above a minimum operating threshold,
- then with internal comparators and logic, determines the sequence of the output supplies,
- finally the X80200 uses internal charge pumps to turn on N-Channel FET pass elements.

The X80200 provides highly flexible power supply turn on options. This flexibility derives from the use of control inputs for each output. The control inputs are based on either a logic level or an adjustable threshold and act directly to drive the gate of the FET or to control the FET after an internal delay period.

The application block diagram (Figure 1) indicates that the VDDH level controls the READY output. Also, the VDDM and VDDL input voltages both need to be above their threshold before the GATE_L and GATE_M FET controls are allowed to turn on. It should also be clear that the GATEH_EN input directly controls the GATE_H output and that the SETV input controls the GATE_L output. The GATE_M output is controlled by either the ENS input or a combination of VFB and REF. Using the ENS input causes the GATE_M output to turn on at a fixed delay time after the GATE_L output. The VFB input allows a feedback voltage to be compared to a reference. When VFB exceeds the reference, GATE_M turns on. The examples presented below demonstrate how this feature is used.

The X80200 also has a 2-wire interface, with three address pins, to allow a processor to remotely shut down the gate voltages and to remotely monitor the status of the gate drives.

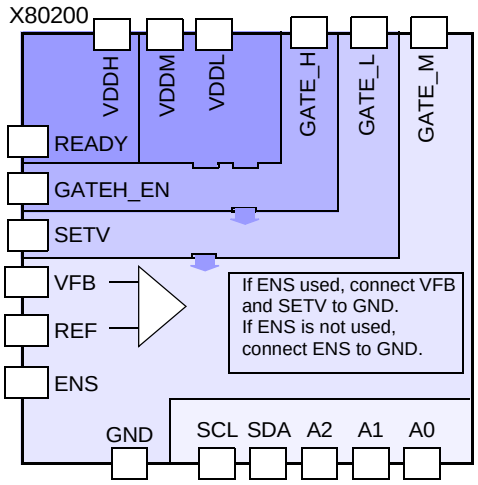

FIGURE 1. APPLICATION BLOCK DIAGRAM OF THE X80200

The X80200 controls three power supplies. For reference, call these VH, VM, and VL for high voltage, medium voltage, and low voltage, respectively. VH is typically the system voltage. In the following examples, this is 5V. VM is typically the I/O voltage. In the examples in this document, VM is 3.3V. VL is typically the core voltage. In the following examples, VL is 2.5V. The X80200 can support a main voltage as low as 3V and I/O and core voltages as low as 1V.

Because of the design of the X80200, the part can be quickly reconfigured for different applications to meet various power sequencing needs. The X80200 offers the choice of time based or voltage based sequencing. To create different sequencing profiles, various sources of signals are used to start the sequencing operation. Additional variations are achieved by delaying the feedback signals or changing the reference voltage on one of the inputs.

The X80200 provides several internal control elements. First, it monitors the three input supplies for undervoltage conditions. The VH output is not turned on until the VH input is above the desired threshold. The VM and VL outputs do not turn on until all three inputs are above the proper threshold. If any fault occurs at the input, the output power supplies are turned off as follows:

- A failure of VH turns off all three outputs.
- A failure of VM turns off VMout, then VLout.
- A failure of VL turns off VMout, then VLout.

To simplify the development of a power sequencing solution, Intersil offers the X80200EVAL kit. This development system simplifies the task of evaluating and testing the X80200 device by providing delay circuits and jumpers from multiple sources to the X80200 inputs. In a voltage based sequencing setup, the board allows the output voltage to power-up in any desired sequence. In a time based sequencing setup, VM and VL (I/O and core voltages) power-up in a core up first, down last configuration; with VH powering up before, during, or after VM and VL. This programming is mainly accomplished with jumpers on the evaluation board, but additional circuitry can be added for more flexibility.

The following examples show sequencing solutions implemented on the X80200EVAL board. Included in the discussion of each solution are specifications for the connections made to each input.

Input Power-up Sequence

For all of the example scenarios in this Application Note, the input voltage sequencing on power-up is identical, as shown in Figure 2.

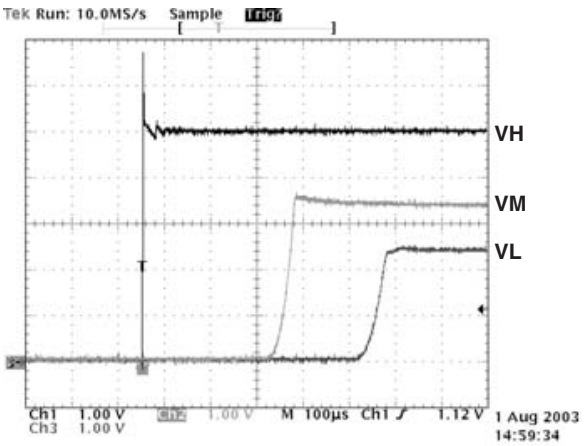

FIGURE 2. INPUT VOLTAGE POWER-UP SEQUENCE

Input Power-down Sequence

Since the X80200 has internal logic to control the power-down sequence of VM and VL, the output power-down sequence is virtually identical, regardless of which input power supply turns off first.

When all of the input supplies turn off together, the input turnoff waveform for the power supplies (in these examples) looks like the one depicted in Figure 3. When the input supplies turn off as shown here, the output supplies are turned off as shown in Figure 4. The speed of output turn off, relative to the input turn off time demonstrates the X80200 active turn off of the FETs. The maintenance of VLout until the other supplies are off shows the effect of the X80200 “core down last” logic.

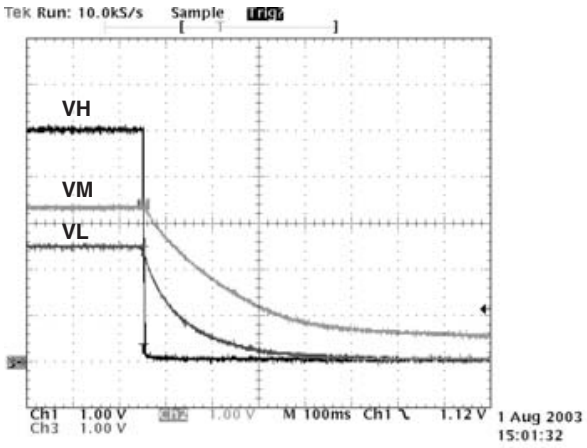

FIGURE 3. INPUT VOLTAGE POWER-DOWN SEQUENCE

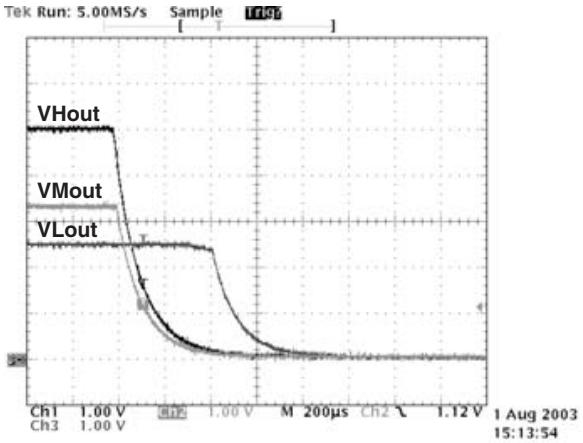

FIGURE 4. OUTPUT POWER-DOWN - ALL SUPPLIES FAil

Each input supply was also turned off separately to evaluate the response to any single input failure. The power-down characteristics of one input supply are not affected by the others remaining on. So, for the following output voltage power-down waveforms, the failing input waveform matches the trace for that supply in Figure 3.

The output power-down sequences are unaffected by the power-up sequencing configuration of the X80200, so these are shown in the next several figures. In these figures, the output power-down waveforms are shown for each individual input supply failing. Figure 5 shows only the 5V input supply failing. Figure 6 shows only the 3.3V input supply failing. Figure 7 shows only the 2.5V input supply failing. In each case, the output core voltage remains ON until the I/O voltage has turned off.

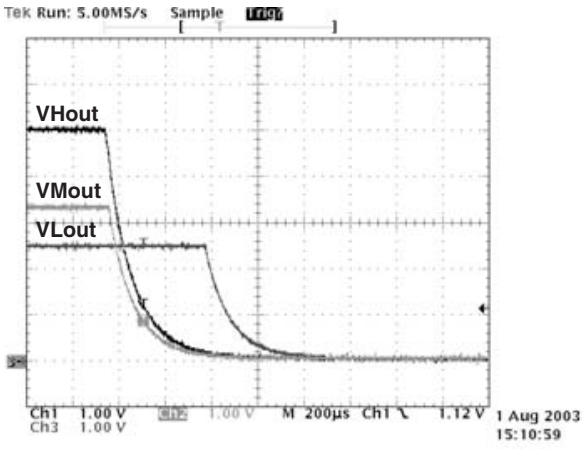

FIGURE 5. OUTPUT POWER-DOWN - 5V ONLY FAILS

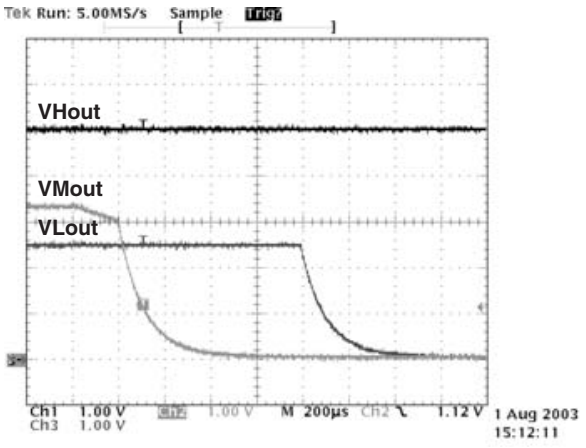

FIGURE 6. OUTPUT POWER-DOWN - 3.3V ONLY FAILS

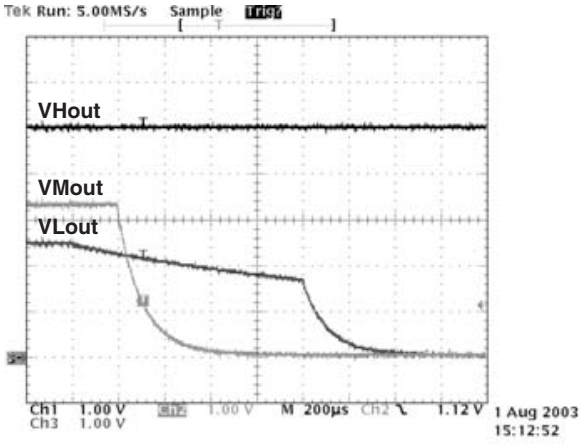

FIGURE 7. OUTPUT POWER-DOWN - 2.5V ONLY FAILS

The X80200 does not automatically control the VH output, unless it is the VHinput that fails. With additional external components, the failure of the core or I/O voltages could be used to “pull down” the open drain READY output of the X80200 to also force the 5V output to turn off.

X80200 Power Sequencing and Interface Circuits

The X80200EVAL board allows sequencing of the power supplies to be controlled by simply using jumpers to select the signals and the timing of the signals that start the charge pumps which turn on the output voltage. For example, the SETV input that turns on the VLout voltage can be controlled from READY, a delayed READY, VHout, or signals indicating that the input power is good. The jumper combinations are shown in the X80200 Evaluation board diagram (Figure 8) following.

N-Channel FETs

The FETs used for these examples are IRF7413 devices from International Rectifier. The FETs need to have some load impedance on the output to operate properly. For the following examples, a parallel combination of a 10kΩ resistor and a 0.1µF capacitor was added to each output. A lower resistance provides a faster turn off of the output.

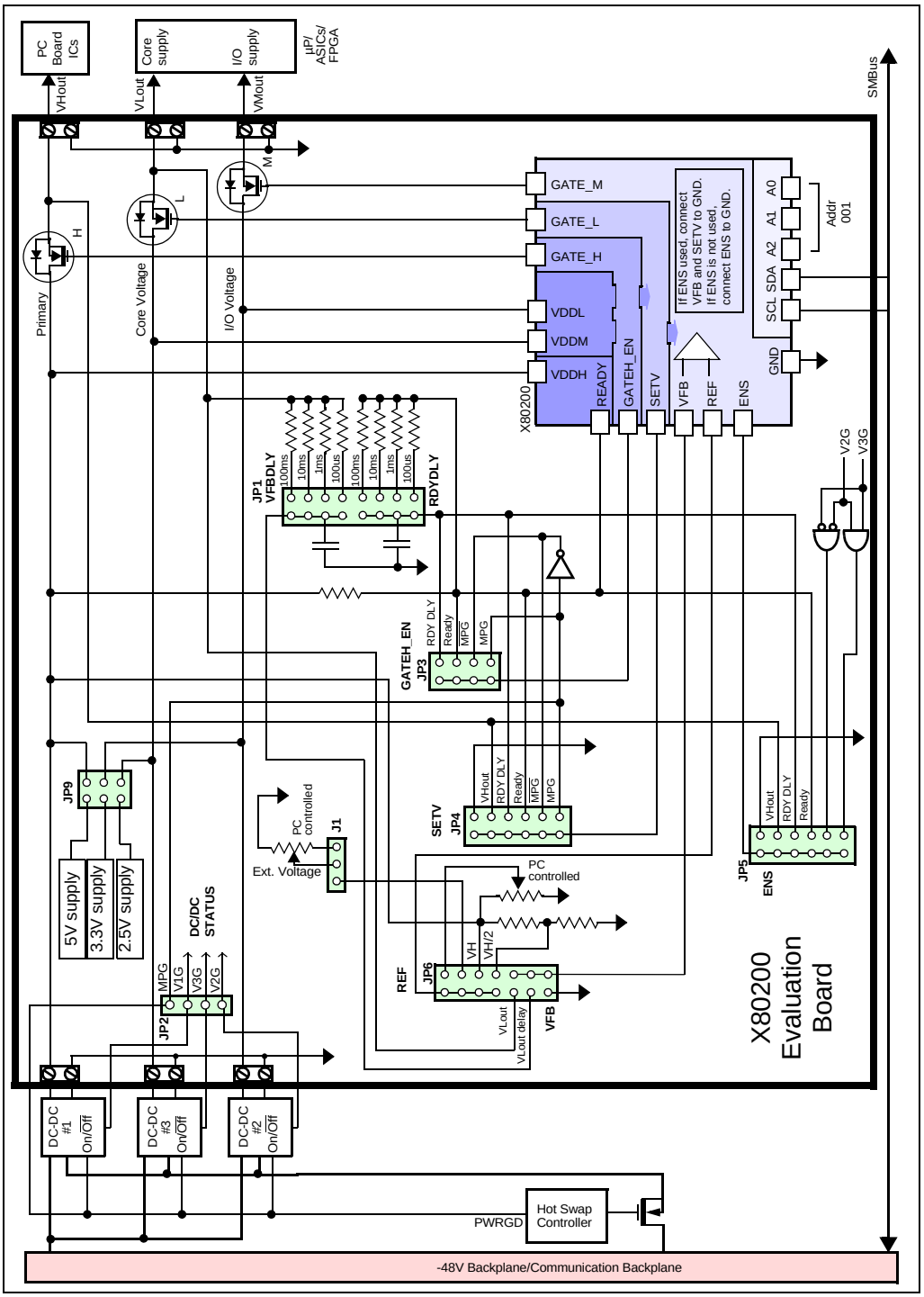

FIGURE 8. X80200 EVALUATION BOARD: JUMPER DIAGRAM

Scenario 1

This example, with connections shown in Figure 9, is a simple voltage sequencer with the main supply powering up first, followed by the Core supply and then the I/O supply. To set this up, GATE_H connects to READY, so as soon as the 5V input supply reaches 4.5V, the READY signal starts the turn on of the 5V output.

SETV connects to VHout, so once VHout reaches a logic ‘1’ the SETV input turns on the core voltage (assuming both the core and I/O input voltages are above their thresholds.)

The VFB input connects to VLout, so as the VLout turns on, it is compared to the REF input. Once VFB exceeds REF, then VMout (the I/O voltage) turns on. Figure 10 and Figure 11 show the power-up timing for two settings for the REF input. This demonstrates the relative timing of the core and I/O turn on. Delaying the VLout feedback to the VFB input pin (using an RC time constant) creates a wider adjustment range.

Scenario 2

For this example, the 5V supply turns on after the core and I/O supplies. To set this up, SETV connects to the READY signal, so so as soon as the 5V supply reaches 4.5V, the ready signal starts the turn on of the core output.

The VFB input connects to VLout, so as the VLout turns on, it is compared to the REF input. Once VFB exceeds REF, then VMout (the I/O voltage) turns on. Figure 13 and Figure 14 show the power-up timing for two settings for the REF input. This demonstrates the relative timing of the core and I/O turn on. Delaying the VLout feedback to the VFB input pin (using an RC time constant) creates a wider adjustment range.

The GATE_H input connects to a delayed READY signal, which is READY delayed by an RC time constant. Once the GATEH_EN input detects that the delayed READY signal is HIGH, the output 5V supply turns on. Changing the RC time constant on the READY signal allows changing the turn on point of the 5V output relative to the core and I/O turn on.

Scenario 3

In scenario 3, the 5V signal turns on first. Then, either the core or I/O turns on, depending on the REF input voltage. To set this up, the GATEH_EN input connects to the READY output, so as soon as the 5V input is good, the 5V output turns on.

The READY signal is delayed by an RC time constant and connected to both the SETV and the VFB inputs. Since the SETV input is a logic level and the VFB input is compared to REF, they have different turn on thresholds. If the REF input is very low, then the I/O output turns on first. At a higher voltage the REF voltage is greater than the SETV input threshold, so the core output voltage turns on first.

The connections for this scenario are shown in Figure 15 The output waveforms are shown in Figure 16, Figure 18, Figure 17, and Figure 19.

Scenario 4

Scenario 4 is a simple time based sequence where READY connects to the GATEH_EN and ENS inputs. As soon as the 5V input supply is good, READY goes active. This turns on the 5V output and (if VM and VL are above their thresholds) starts the core and I/O power-up sequence. The main voltage powers up first, followed by the core voltage. Then, a fixed delay after the core turns on, the I/O voltage powers up.

The connections for this scenario are shown in Figure 20 and the timing waveform is in Figure 21.

Scenario 5

This scenario is identical to Scenario 4, except the ENS input is delayed by an RC time constant. It shows that the relative timing of the 5V and core and I/O voltages is easily changed.

See Figure 22 for the connections for this circuit and Figure 23 for the power-up timing.

Summary

The X80200 is a highly flexible building block for meeting virtually any sequencing need. Typically this sequencing is required for some of the new high performance processors and DSPs, but sequencing may also be needed for managing power consumption, sequencing peripherals or for other needs. This application note shows many different power supply sequencing options and provides the connections necessary to recreate the timing sequences.

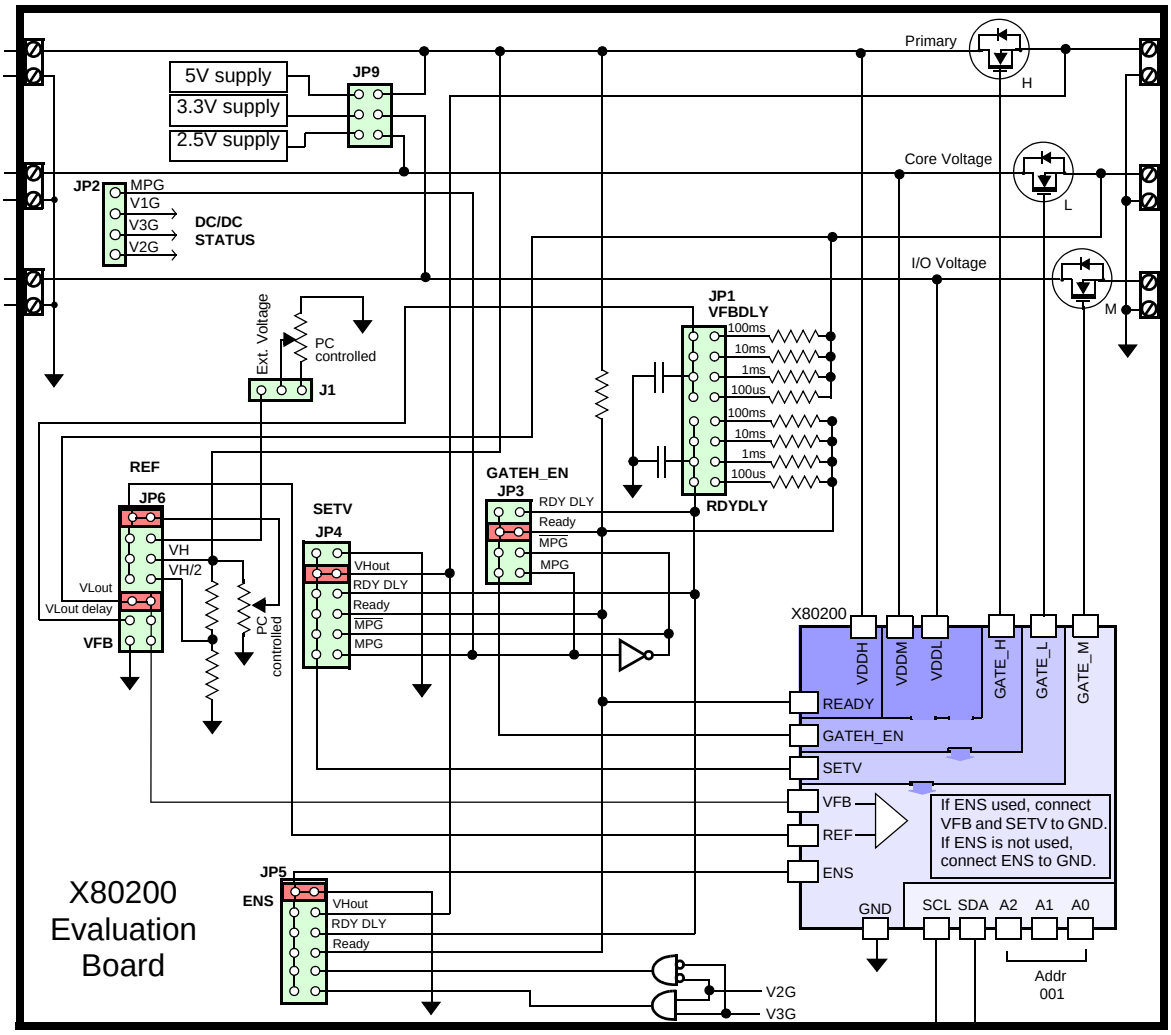

FIGURE 9. SCENARIO 1: VH, VL, VM SIMPLE VOLTAGE-BASED SEQUENCE

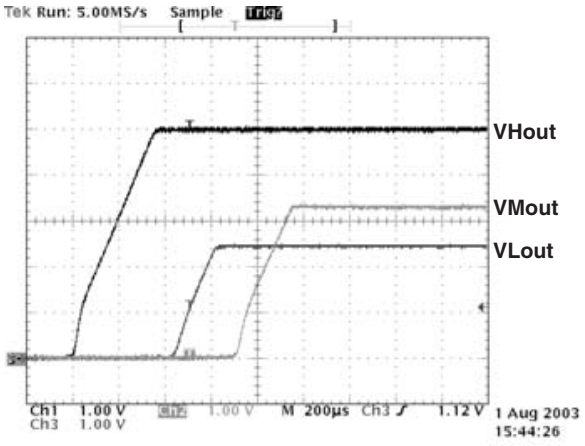

FIGURE 10. SCENARIO 1 POWER-UP WAVEFORM (REF = 0V)

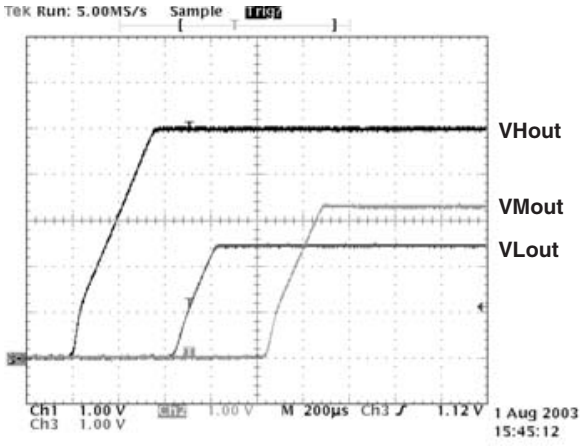

FIGURE 11. SCENARIO 1 POWER-UP WAVEFORM (REF = 2.25V)

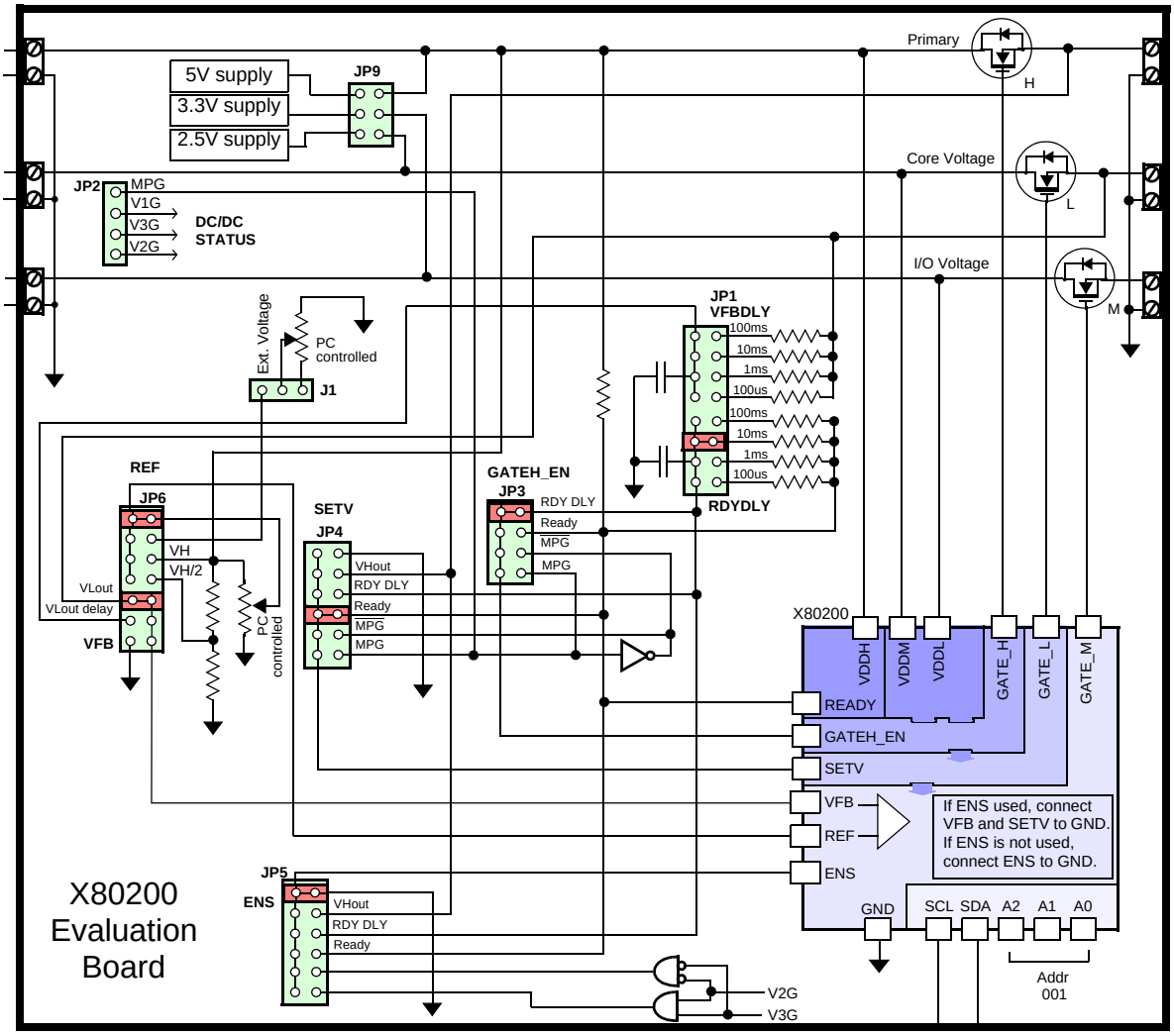

FIGURE 12. SCENARIO 2: VL, VM, VH SIMPLE VOLTAGE-BASED SEQUENCE

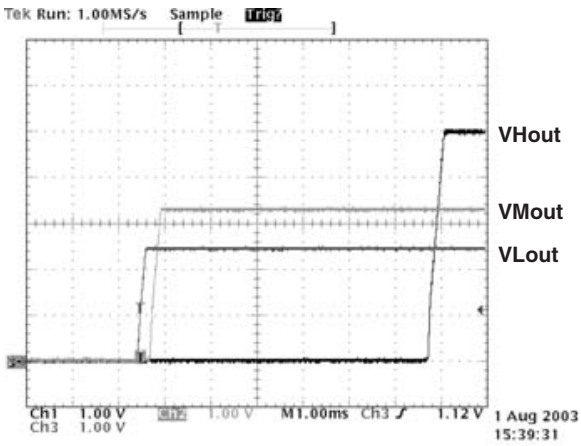

FIGURE 13. SCENARIO 2 POWER-UP WAVEFORM (REF = 0V)

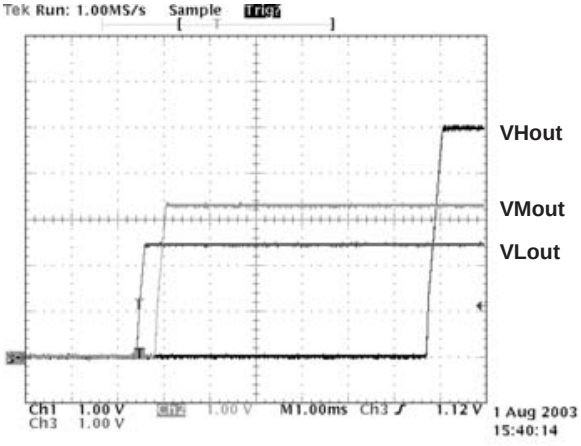

FIGURE 14. SCENARIO 2 POWER-UP WAVEFORM (REF = 2.25V)

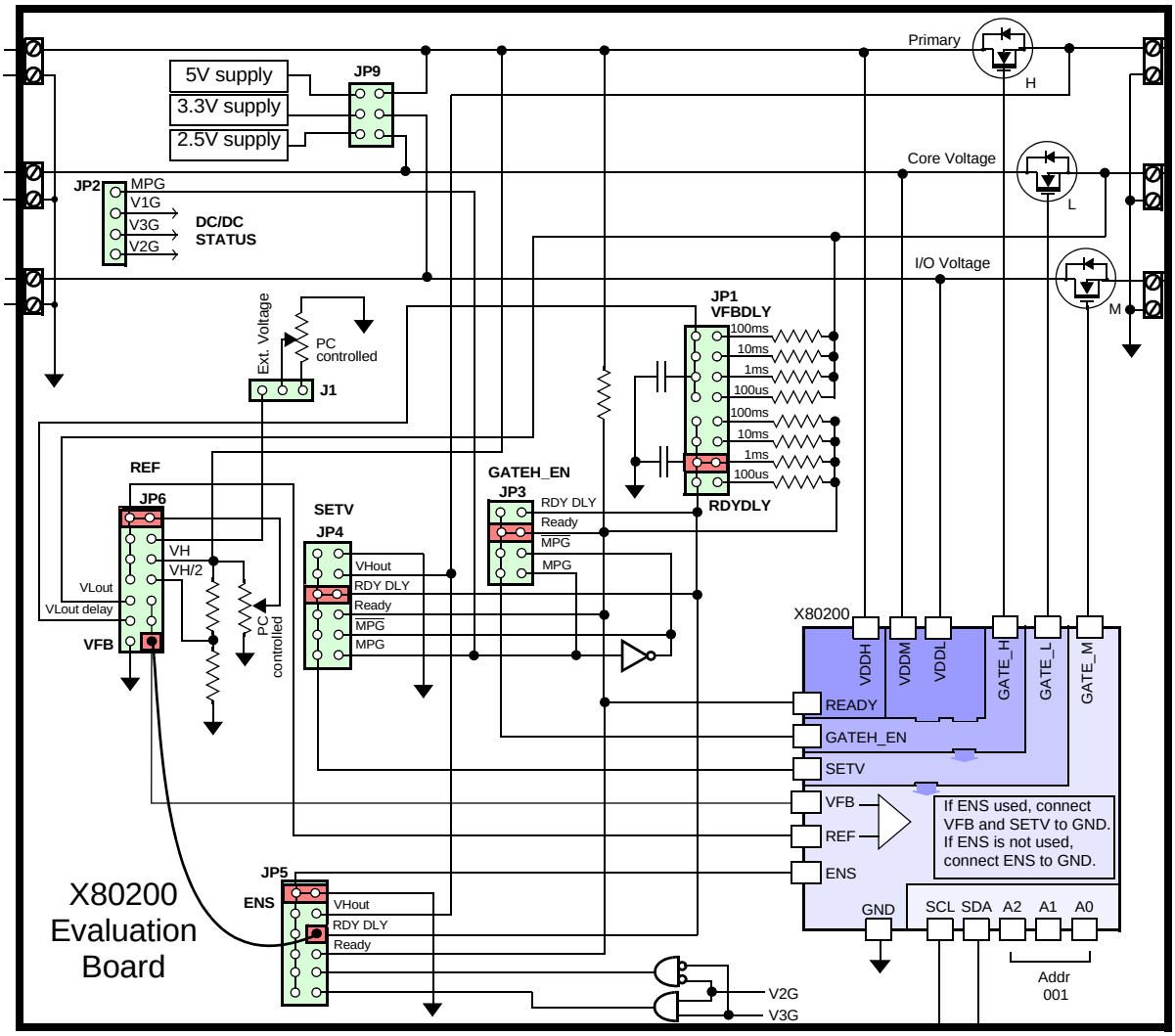

FIGURE 15. SCENARIO 3: VH, VL, VM SEQUENCE WITH VARIABLE VM TIMING

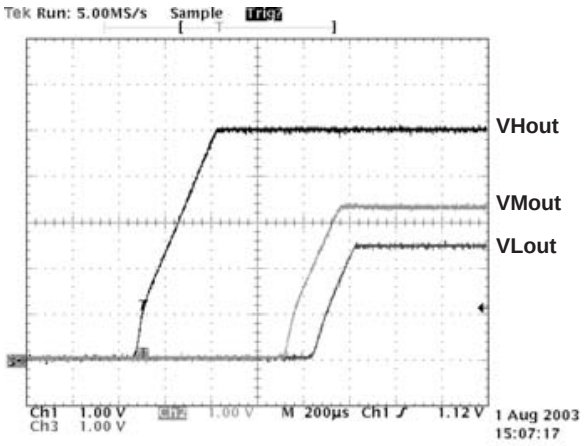

FIGURE 16. SCENARIO 3 POWER-UP WAVEFORM (REF = 0V)

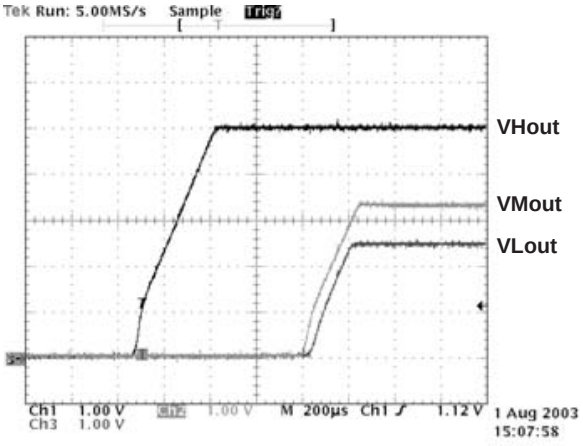

FIGURE 18. SCENARIO 3 POWER-UP WAVEFORM (REF = 2.45V)

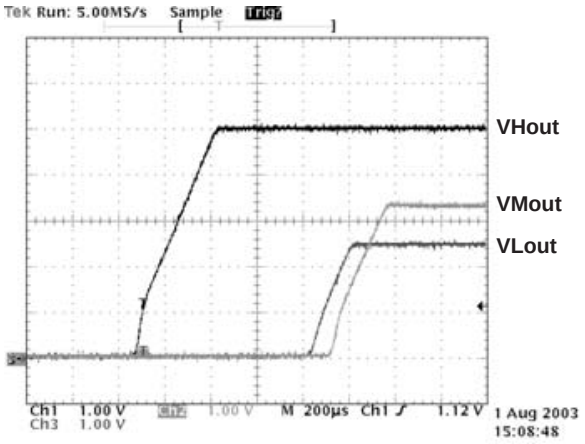

FIGURE 17. SCENARIO 3 POWER-UP WAVEFORM (REF = 2.55V)

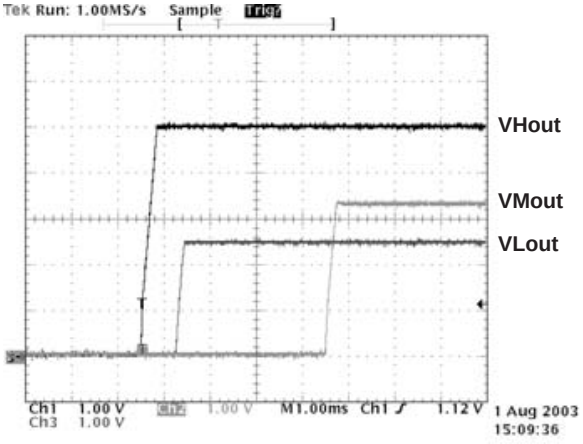

FIGURE 19. SCENARIO 3 POWER-UP WAVEFORM (REF = 4.5V)

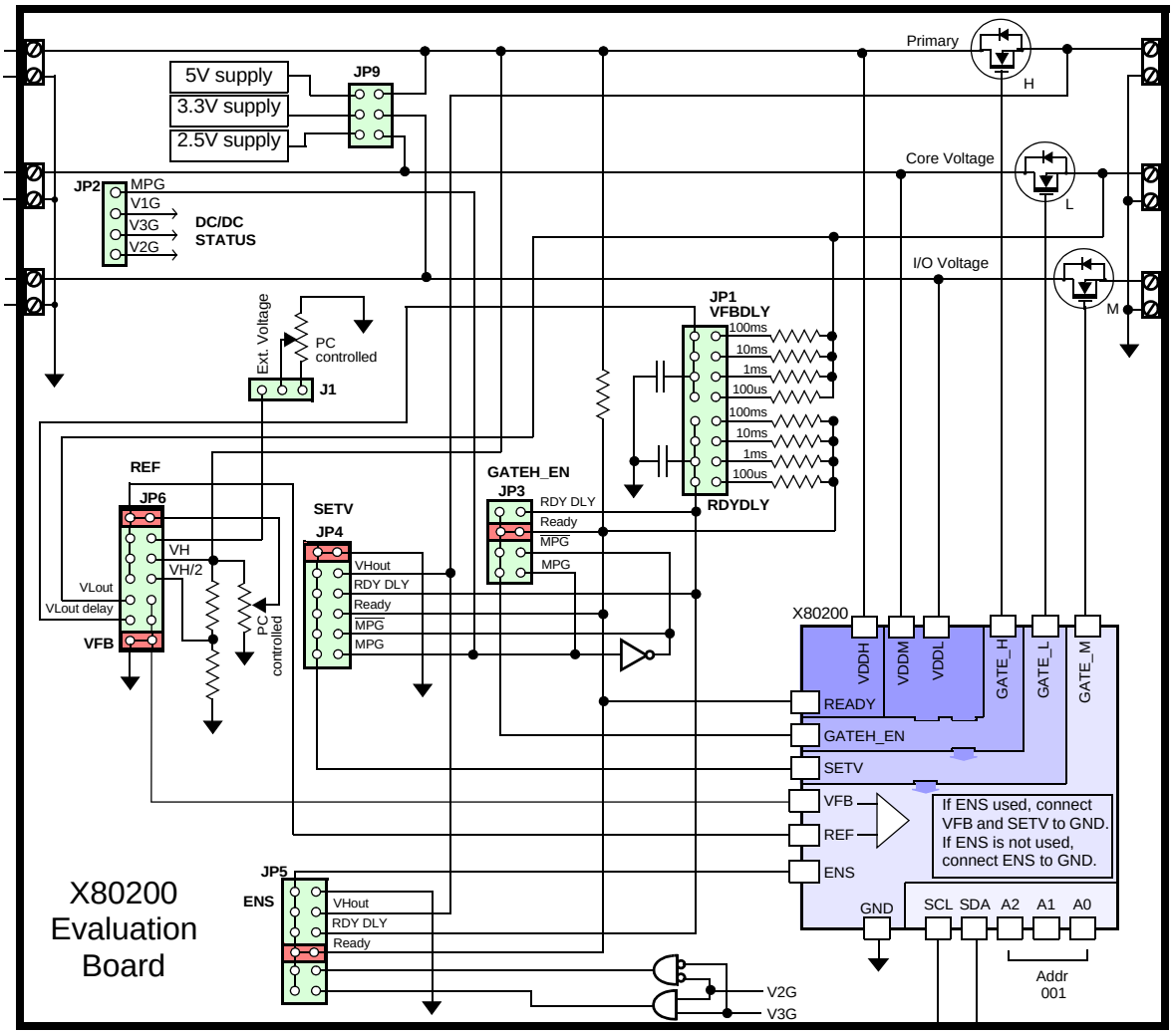

FIGURE 20. SCENARIO 4: VH, VL, VM SIMPLE TIME-BASED SEQUENCE

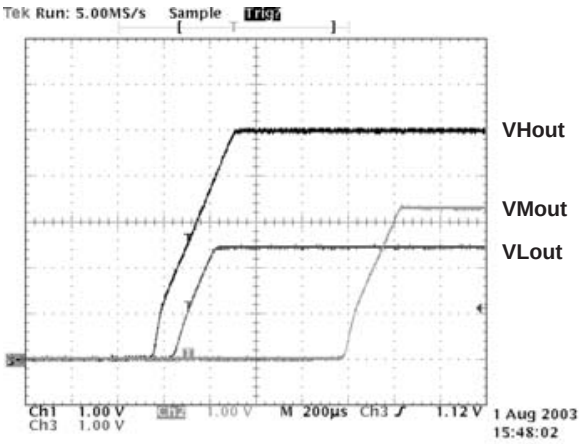

FIGURE 21. SCENARIO 4 POWER-UP WAVEFORM

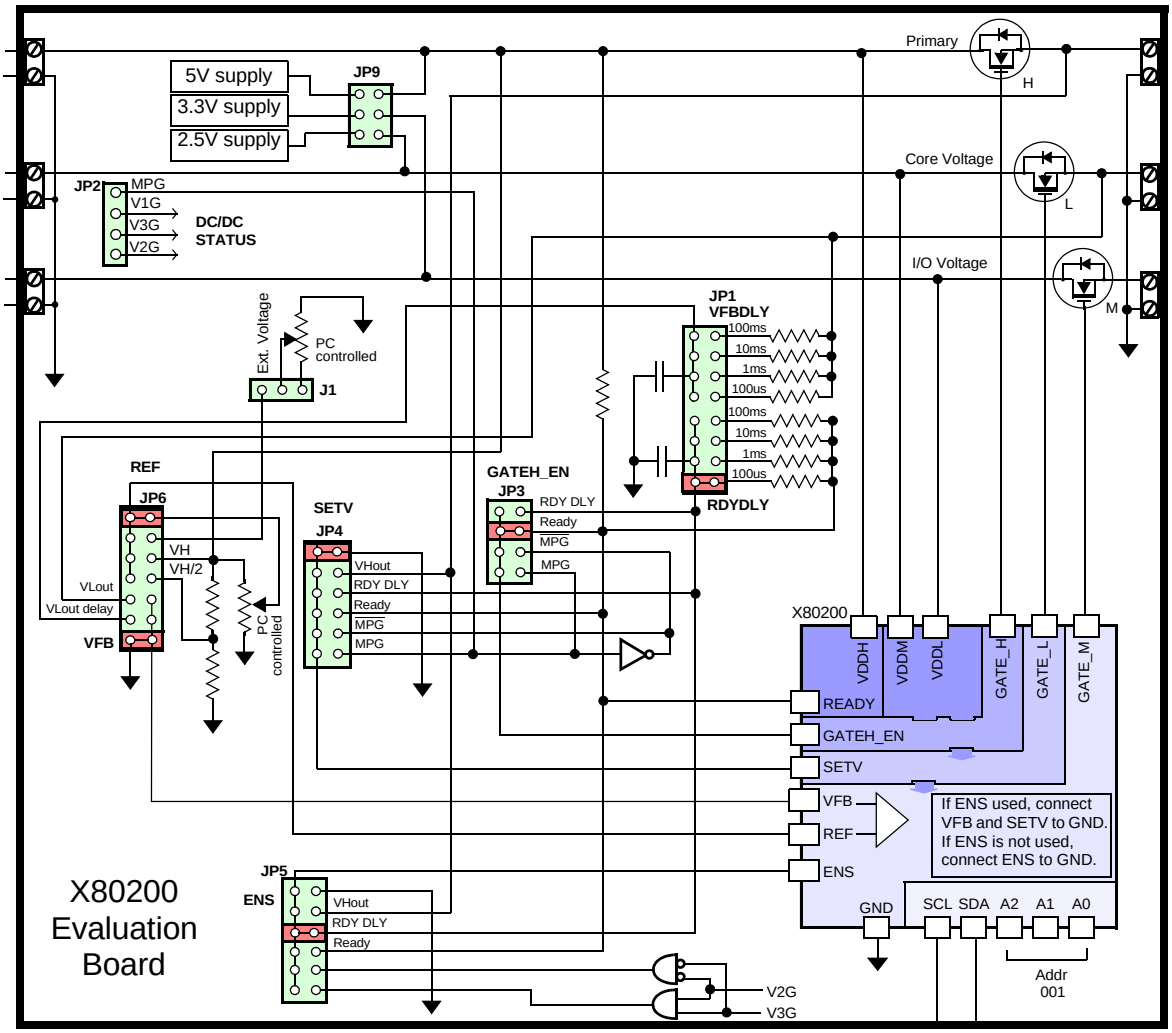

FIGURE 22. SCENARIO 5: VH, VL, VM SIMPLE TIME-BASED SEQUENCE (USING DELAYED READY)

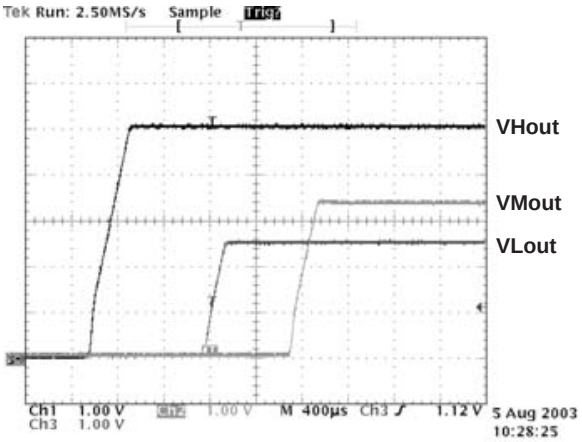

FIGURE 23. SCENARIO 5 POWER-UP WAVEFORM